REMARKS

By this Amendment, claims 1-3, 5-7, 9-11, and 13-19 have been amended to more appropriately claim the invention. As a result of this Amendment, claims 1-19 remain pending. No new matter has been added.

As required by 37 C.F.R. § 1.121(c)(1)(ii), Applicant provides a marked-up version of the amended claims 1-3, 5-7, 9-11, and 13-19 in the attached Appendix.

In the previous Office Action, claims 1-19 were rejected under 35 U.S.C. §102(e) as anticipated by U.S. Patent No. 6,140,832 to *Vu et al.* Applicant respectfully traverses these rejections because *Vu* fails to anticipate claims 1-19 for the following reasons.

To anticipate claims 1-19 under 35 U.S.C. §102(e), *Vu*, taken individually, must explicitly or inherently disclose each and every element recited in the claims 1-19 of the present invention. *See* M.P.E.P. § 2131 (8th Ed. 2001).

Vu describes an integrated circuit device screening method that uses "IDDQ testing to screen out defective integrated circuit devices." *See* col. 1, ll. 4-7. *Vu* employs a computer-implemented method to generate an indication of "whether IDDQ values associated with integrated circuits that have been tested are within the IDDQ specification or not." *See* Abstract.

Independent claim 1 is directed to a "semiconductor testing apparatus for testing semiconductor devices, configured to feed back data of returned samples which have been shipped as good samples, but returned from a user to a manufacture as faulty samples" comprising, *inter alia,* "an IDDQ measuring circuit configured to measure

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current data of good samples and the returned samples, by supplying test vector data to the good and returned samples" and "a determination circuit configured to determine a range of pass/fail decision criteria and effective address pairs for testing target semiconductor devices based upon the measured current data."

In contrast, *Vu* relies on a computer program to extract data derived from the IDDQ functional tests and to compute minimum and maximum current leakage limits based upon a parametric test. *See* col. 2, ll. 8-14. In particular, *Vu* uses computer program 20 to determine the lot specification "minimum and maximum current leakage limits for the integrated circuit based upon data derived from the parametric test 21 for that particular lot." *See* col. 3, ll. 34-37.

Nowhere does *Vu's* method of screening out defective integrated circuit devices mention at least a "semiconductor testing apparatus for testing semiconductor devices, configured to feed back data of returned samples which have been shipped as good samples, but returned from a user to a manufacture as faulty samples," as recited in claim 1.

Further, *Vu* also fails to disclose or suggest "an IDDQ measuring circuit configured to measure current data of good samples and the returned samples, by supplying test vector data to the good and returned samples" and "a determination circuit configured to determine a range of pass/fail decision criteria and effective address pairs for testing target semiconductor devices based upon the measured current data," as recited in claim 1. For at least these reasons, claim 1 is not anticipated

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by *Vu* and Applicant respectfully requests that the rejection under 35 U.S.C. §102(e) of claim 1 be withdrawn.

Claims 2-4 depend from allowable claim 1 and include all the elements thereof. Therefore, claims 2-4 are allowable at least based on such dependency.

Independent claim 5 is directed to a "semiconductor testing method for testing semiconductor devices, configured to feed back data of returned samples which have been shipped as good samples, but returned from a user to a manufacture as faulty samples so as to improve testing performance," comprising, *inter alia,* "measuring current data of good samples and the returned samples by supplying the test vector data to the good and returned samples" and "determining a range of pass/fail decision criteria and effective address pairs for testing target semiconductor devices based upon the measured current data."

For the reasons discussed above with respect to independent claim 1, *Vu* fails to disclose or suggest at least a "semiconductor testing method for testing semiconductor devices, configured to feed back data of returned samples which have been shipped as good samples, but returned from a user to a manufacture as faulty samples so as to improve testing performance," as recited in claim 5.

In addition, as discussed above with respect to independent claim 1, *Vu* also fails to disclose or suggest "measuring current data of good samples and the returned samples by supplying the test vector data to the good and returned samples" and "determining a range of pass/fail decision criteria and effective address pairs for testing

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target semiconductor devices based upon the measured current data," as recited in claim 5. For at least these reasons, claim 5 is not anticipated by *Vu* and Applicant respectfully requests that the rejection under 35 U.S.C. §102(e) of claim 5 be withdrawn.

Claims 6-8 depend from allowable claim 5 and include all the elements thereof. Therefore, claims 6-8 are allowable at least based on such dependency.

Independent claim 9 is directed to "a program with which a semiconductor testing method is executed in a semiconductor testing apparatus which comprises a read circuit, a determination circuit, an IDDQ measuring circuit configured to test semiconductor devices by applying test vector data, configured to feed back data of returned samples which have been shipped as good samples, but returned from a user to a manufacture as faulty samples so as to improve testing performance," the program comprising, *inter alia,* "instructions configured to measure current data of the good and returned samples" and "instructions configured to determine a range of pass/fail decision criteria and effective address pairs for testing target semiconductor devices based upon the measured current data."

Again, for the reasons discussed above with respect to independent claim 1, *Vu* fails to disclose or suggest at least "an IDDQ measuring circuit configured to test semiconductor devices by applying test vector data, configured to feed back data of returned samples which have been shipped as good samples, but returned from a user

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to a manufacture as faulty samples so as to improve testing performance," as recited in claim 9.

Further, *Vu* also fails to disclose or suggest "instructions configured to measure current data of the good and returned samples" and "instructions configured to determine a range of pass/fail decision criteria and effective address pairs for testing target semiconductor devices based upon the measured current data," as recited in claim 9. Therefore, for at least these reasons, claim 9 is not anticipated by *Vu* and Applicant respectfully requests that the rejection under 35 U.S.C. §102(e) of claim 9 be withdrawn.

Claims 10-12 depend from allowable claim 9 and include all the elements thereof. Therefore, claims 10-12 are allowable at least based on such dependency.

Independent claim 13 is directed to a "semiconductor testing method of specifying a faulty part in a semiconductor device, configured to feed back data of returned samples which have been shipped as good samples, but returned from a user to a manufacture as faulty samples so as to improve testing performance," the method comprising, *inter alia,* "measuring current data of the good and returned samples, employing an IDDQ measuring circuit" and "determining a range of pass/fail decision criteria and effective address pairs for testing target semiconductor devices in a manufacturing process based upon the measured current data."

Similarly, for the reasons discussed above with respect to independent claim 1, *Vu* fails to disclose or suggest at least "a semiconductor testing method of specifying a

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faulty part in a semiconductor device, configured to feed back data of returned samples which have been shipped as good samples, but returned from a user to a manufacture as faulty samples so as to improve testing performance," as recited in claim 13.

In addition, *Vu* also fails to disclose or suggest "measuring current data of the good and returned samples, employing an IDDQ measuring circuit" and "determining a range of pass/fail decision criteria and effective address pairs for testing target semiconductor devices in a manufacturing process based upon the measured current data," as recited in claim 13. Therefore, for at least these reasons, claim 13 is not anticipated by *Vu* and Applicant respectfully requests that the rejection under 35 U.S.C. §102(e) of claim 13 be withdrawn.

Claims 14-15 and 17-18 depend from allowable claim 13 and include all the elements thereof. Therefore, claims 14-15 and 17-18 are allowable at least based on such dependency.

Independent claim 16 is directed to a "semiconductor testing apparatus for specifying a faulty part in a semiconductor device, configured to feed back data of returned samples which have been shipped as good samples, but returned from a user to a manufacture as faulty samples so as to improve testing performance" comprising, *inter alia,* "an IDDQ measuring circuit configured to measure current data of good samples and the returned samples, by supplying the test vector data to the good and returned samples" and "a determination circuit configured to determine a range of

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pass/fail decision criteria and effective address pairs for testing target semiconductor devices in a manufacturing process."

Likewise, for the reasons discussed above with respect to independent claim 1, *Vu* fails to disclose or suggest at least "a semiconductor testing apparatus for specifying a faulty part in a semiconductor device, configured to feed back data of returned samples which have been shipped as good samples, but returned from a user to a manufacture as faulty samples so as to improve testing performance," as recited in claim 16.

Vu also fails to disclose or suggest "an IDDQ measuring circuit configured to measure current data of good samples and the returned samples, by supplying the test vector data to the good and returned samples" and "a determination circuit configured to determine a range of pass/fail decision criteria and effective address pairs for testing target semiconductor devices in a manufacturing process," as recited in claim 16. Therefore, for at least these reasons, claim 16 is not anticipated by *Vu* and Applicant respectfully requests that the rejection under 35 U.S.C. §102(e) of claim 16 be withdrawn.

Independent claim 19 is directed to "a program with which a semiconductor testing method is executed by a computer in a semiconductor testing apparatus which comprises a read circuit, a determination circuit, and a faulty part specifying circuit, configured to feed back data of returned samples which have been shipped as good samples, but returned from a user to a manufacture as faulty samples so as to improve

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testing performance," the program comprising, *inter alia* "instructions configured to measure current data of good samples and the returned samples, employing an IDDQ measuring circuit, by supplying the test vector data to good and returned samples" and "instructions configured to determine a range of pass/fail decision criteria and effective address pairs for testing target semiconductor devices in a manufacturing process based upon the measured data."

Again, for the reasons discussed above with respect to independent claim 1, *Vu* fails to disclose or suggest at least "a program with which a semiconductor testing method is executed by a computer in a semiconductor testing apparatus which comprises a read circuit, a determination circuit, and a faulty part specifying circuit, configured to feed back data of returned samples which have been shipped as good samples, but returned from a user to a manufacture as faulty samples so as to improve testing performance."

In addition, *Vu* also fails to disclose or suggest "instructions configured to measure current data of good samples and the returned samples, employing an IDDQ measuring circuit, by supplying the test vector data to good and returned samples" and "instructions configured to determine a range of pass/fail decision criteria and effective address pairs for testing target semiconductor devices in a manufacturing process based upon the measured data," as recited in claim 19. Therefore, for at least these reasons, claim 19 is not anticipated by *Vu* and Applicant respectfully requests that the rejection under 35 U.S.C. §102(e) of claim 19 be withdrawn.

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In view of the foregoing amendments and remarks, Applicant respectfully requests the reconsideration and reexamination of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

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Dated: July 18, 2003

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APPENDIX TO AMENDMENT OF JULY 18, 2003
VERSION WITH MARKINGS TO SHOW CHANGES MADE

AMENDMENTS TO THE CLAIMS

Please amend claims 1-3, 5-7, 9-11, and 13-19 as follows:

1. (Twice Amended) A semiconductor testing apparatus for testing semiconductor devices, configured to feed back data of returned samples which have been shipped as good samples, but returned from a user to a manufacture as faulty samples so as to improve testing performance, the semiconductor testing apparatus comprising:

[a read] an IDDQ measuring circuit configured to [read measurement data including a test vector data and] measure current data of good samples and [data of faulty samples returned to a manufacturer] the returned samples, by supplying test vector data to the good and returned samples;

a determination circuit configured to [supply the test vector data to the good samples and faulty samples, and to] determine a range of pass/fail decision criteria and effective address pairs for testing target semiconductor devices based upon the measured current data [; and] ,

[an] wherein the IDDQ measuring circuit [configured to test] tests the target semiconductor devices by applying the [effective] test vector data for the effective address pairs.

2. (Twice Amended) The apparatus of claim 1 wherein the determination circuit comprises:

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a changing rate calculation circuit configured to select a plurality of address pairs from the test vector data, to supply the address pairs to the good samples and the [faulty] returned samples, to measure current-values of the good samples and [faulty] returned samples, and to calculate changing rates of each of the good samples and [faulty] returned samples;

a range criteria determination circuit configured to determine [a] the range of pass/fail decision criteria by using the changing rates of each of the good samples;

a comparing circuit configured to compare the changing rates of each of the [faulty] returned samples to the range of pass/fail decision criteria, and to determine whether the changing rates of each of the [faulty] returned samples fall outside of the range of pass/fail decision criteria; and

an effective address pair determination circuit configured to determine the changing rate falling out of the range of pass/fail decision criteria, and to select an address pair which makes the [faulty] returned samples to provide the changing rate falling outside of the range of the pass/fail decision criteria as [an] the effective address pair.

3. (Twice Amended) The apparatus of claim 1, wherein the IDDQ measuring circuit comprises:

a tester configured to: acquire the effective address pair, supply the test [vectors] data corresponding to the effective address pair to the target

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semiconductor device, measure current-value output of the target semiconductor device, and calculate changing rates of the target semiconductor device; and

a decision circuit configured to determine a changing rate falling outside of the range of pass/fail decision criteria.

5. (Thrice Amended) A semiconductor testing method for testing semiconductor devices, configured to feed back data of returned samples which have been shipped as good samples, but returned from a user to a manufacture as faulty samples so as to improve testing performance, the method comprising:

reading [measurement data of an IDDQ measuring circuit configured to test semiconductor devices by applying an effective] test vector data [,including a test vector data and];

measuring current data of good samples and [faulty samples returned to a manufacturer] the returned samples [;] by supplying the test vector data to the good [samples] and [the faulty] returned samples;

determining a range of pass/fail decision criteria and effective address pairs for testing target semiconductor devices based upon the measured current data; and

applying the test [vectors of] vector data for the effective address pairs to the target semiconductor devices for testing.

6. (Twice Amended) The method of claim 5, further comprising:

selecting a plurality of address pairs from the test vector data;

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supplying the address pairs to the good samples and the [faulty] returned samples;

measuring current-values of the good samples and the [faulty] returned samples;

calculating changing rates of each of the good samples and the [faulty] returned samples;

determining a range of pass/fail decision criteria by using the changing rates of each of the good samples;

comparing the changing rates of each of the [faulty] returned samples to the range of pass/fail decision criteria;

determining whether the changing rates of each of the [faulty] returned samples fall outside of the range of pass/fail decision criteria;

determining the changing rate falling out side of the range of pass/fail decision criteria; and

selecting an address pair which makes the [faulty] returned samples to provide the changing rate falling outside of the range of pass/fail decision criteria as [an] the effective address pair.

7. (Twice Amended) The method of claim 5, further comprising:

acquiring the effective address pair;

supplying the test [vectors] vector data corresponding to the effective address pair to the target semiconductor devices;

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measuring current-value output of the target semiconductor devices;

calculating change rates of the target semiconductor devices; and

determining a changing rate falling outside of the range of pass/fail decision criteria.

9. (Thrice Amended) A program with which a semiconductor testing method is executed by a computer in a semiconductor testing apparatus which comprises a read circuit, a determination circuit, an IDDQ measuring circuit configured to test semiconductor devices by applying [an effective] test vector data, configured to feed back data of returned samples which have been shipped as good samples, but returned from a user to a manufacture as faulty samples so as to improve testing performance, the program comprising:

instructions configured to read [measurement data, including a] the test vector data [and data of good samples and faulty samples returned to a manufacturer];

instructions configured to supply the test vector data to good samples and [faulty] returned samples;

instructions configured to measure current data of the good and returned samples;

instructions configured to determine a range of pass/fail decision criteria and effective address pairs for testing target semiconductor devices based upon the measured current data; and

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instructions configured to apply the test [vectors of] vector data for the effective address pairs for testing.

10. (Twice Amended) The program of claim 9, further comprising:

instructions configured to select a plurality of address pairs from the test vector data;

instructions configured to supply the address pairs to the good samples and the [faulty] returned samples;

instructions configured to measure current-values of the good samples and the [faulty] returned samples;

instructions configured to calculate changing rates of each of the good samples and the [faulty] returned samples;

instructions configured to determine a range of pass/fail decision criteria by using the changing rates of each of the good samples;

instructions configured to compare the changing rates of each of the [faulty] returned samples to the range of pass/fail decision criteria;

instructions configured to determine whether the changing rates of each samples fall outside of the range of pass/fail decision criteria;

instructions configured to determine the changing rate falling outside of the range of pass fail decision criteria; and

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instructions configured to select an address pair that makes the [faulty] returned samples to provide the changing rate falling outside of the range of pass/fail decision criteria as [an] the effective address pair.

11. (Twice Amended) The program of claim 9, further comprising:

instructions configured to acquire the effective address pair;

instructions configured to supply the test [vectors] vector data corresponding to the effective address pair to the target semiconductor devices;

instructions configured to measure current-value output of the target semiconductor devices;

instructions configured to calculate changing rates of the target semiconductor devices; and

instructions configured to determine a changing rate falling outside of the range of pass/fail decision criteria.

13. (Thrice Amended) A semiconductor testing method of specifying a faulty part in a semiconductor device, configured to feed back data of returned samples which have been shipped as good samples, but returned from a user to a manufacture as faulty samples so as to improve testing performance, the method comprising:

reading [measurement data of an IDDQ measuring circuit configured to test semiconductor devices by applying an effective test vector, wherein the measurement data includes] a test program [,] and test vector data [, data of good samples and faulty samples returned to a manufacturer];

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supplying the test vector data to good and [faulty] returned samples;

measuring current data of the good and returned samples, employing an IDDQ measuring circuit;

determining a range of pass/fail decision criteria and effective address pairs for testing target semiconductor devices in a manufacturing process based upon the measured current data;

applying the test [vectors of] vector data for the effective address pairs to a target semiconductor device; and

specifying a faulty part within the target semiconductor device by measuring an emission from the target semiconductor device.

14. (Twice Amended) The method of claim 13, further comprising:

selecting a plurality of address pairs from the test vector data;

supplying the address pairs to the good samples and the [faulty] returned samples;

measuring current-values of the good samples and [faulty] returned samples;

calculating changing rates of each of the good samples and [faulty] returned samples;

determining a range of pass/fail decision criteria by using the changing rates of each of the good samples;

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comparing the changing rates of each of the [faulty] returned samples to the range of pass/fail decision criteria;

determining whether the changing rates of each of the [faulty] returned samples fall outside of the range of pass/fail decision criteria;

determining the changing rate falling outside of the range of pass/fail decision criteria; and

selecting an address pair which makes the [faulty] returned samples to provide the changing rate falling outside of the range of pass/fail decision criteria as [an] the effective address pair.

15. (Twice Amended) The method of claim 14, wherein the faulty part specifying step further comprises:

acquiring the effective address pair;

supplying the test [vectors] vector data corresponding to the effective address pair to the target semiconductor device;

measuring current-value output of the target semiconductor device;

calculating changing rates of the target semiconductor device;

measuring an emission from the target semiconductor device; and

determining a changing rate falling outside of the range of pass/fail decision criteria.

16. (Thrice Amended) A semiconductor testing apparatus for specifying a faulty part in a semiconductor device, configured to feed back data of returned samples

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which have been shipped as good samples, but returned from a user to a manufacture as faulty samples so as to improve testing performance, the apparatus comprising:

a read circuit configured to read test vector data and a test program [measurement data of];

an IDDQ measuring circuit configured to [test semiconductor devices by applying an effective test vector, wherein the measurement] measure current data [includes a test program, test vector data, data] of good samples and [faulty samples returned to a manufacturer] the returned samples, by supplying the test vector data to the good and returned samples;

a determination circuit configured to [supply the test vector data to the good samples and faulty samples, and to] determine a range of pass/fail decision criteria and effective address pairs for testing target semiconductor devices in a manufacturing process; and

a faulty part specifying circuit configured to apply the test [vectors of] vector data for the effective address pairs to [a] the target semiconductor device and to specify a faulty part by measuring an emission from the target semiconductor device.

17. (Twice Amended) The method of claim 13, wherein determining a range of pass/fail decision criteria is achieved by:

a changing rate calculation circuit configured to select a plurality of address pairs from the test vector data, to supply the address pairs to the good

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samples and the [faulty] returned samples, to measure current-values of the good samples and [faulty] returned samples, and to calculate changing rates of each of the good samples and [faulty] returned samples;

a range criteria determination circuit configured to determine a range of pass/fail decision criteria by using the changing rates of each of the good samples;

a comparing circuit configured to compare the changing rates of each of the [faulty] returned samples to the range of pass/fail decision criteria, and to determine whether the changing rates of each of the [faulty] returned samples fall outside of the range of pass/fail decision criteria; and

an effective address pair determination circuit configured to determine the changing rate falling outside of the range of pass/fail decision criteria, and to select an address pair that makes the [faulty] returned samples to provide the changing rate falling outside of the range of pass/fail decision criteria as an effective address pair.

18. (Twice Amended) The method of claim 17, wherein the faulty part specifying circuit further comprises:

a tester configured to acquire the effective address pair, to supply the test [vectors] vector data corresponding to the effective address pair to the target semiconductor device, to measure current-value output of the target

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semiconductor device, and to calculate changing rates of the target semiconductor device;

an emission measuring circuit configured to measure an emission from the target semiconductor device; and

a decision circuit configured to determine a changing rate falling outside of the range of pass/fail decision criteria.

19. (Thrice Amended) A program with which a semiconductor testing method is executed by a computer in a semiconductor testing apparatus which comprises a read circuit, a determination circuit, and a faulty part specifying circuit, configured to feed back data of returned samples which have been shipped as good samples, but returned from a user to a manufacture as faulty samples so as to improve testing performance, the program comprising:

instructions configured to read [measurement data of an IDDQ measuring circuit configured to test semiconductor devices by applying an effective test vector, wherein the measurement data includes] a test program [,] and test vector data [, data of good samples and faulty samples returned to a manufacturer];

instructions configured to measure current data of good samples and the returned samples, employing an IDDQ measuring circuit, by [supply] supplying the test vector data to good [samples] and [faulty] returned samples;

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instructions configured to determine a range of pass/fail decision criteria and effective address pairs for testing target semiconductor devices in a manufacturing process based upon the measured data;

instructions to apply the test [vectors of] vector data for the effective address pairs to [a] the target semiconductor device; and

instructions to specify a faulty part within the target semiconductor device by measuring an emission from the target semiconductor device.

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